UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/689,486	10/21/2003	Tatsuya Kanda	108397-00110	7757

4372 7590 11/07/2005

ARENT FOX PLLC
1050 CONNECTICUT AVENUE, N.W.
SUITE 400
WASHINGTON, DC 20036

EXAMINER	
SONG, JASMINE	
ART UNIT	**PAPER NUMBER**
2188	

DATE MAILED: 11/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/689,486	KANDA ET AL.	
	Examiner	Art Unit	
	Jasmine Song	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *6-10* is/are allowed.

6)☒ Claim(s) *1,2 and 5* is/are rejected.

7)☒ Claim(s) *3 and 4* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/21/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

Specification

1. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Drawings

2. The drawings filed on 10/21/2003 have been approved by the Examiner.

Oath/Declaration

3. The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in 37 C.F.R. 1.63.

Priority

4. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

5. The information disclosure statement (IDS) submitted on 10/21/2003 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Title

6. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1-2 and 5 rejected under 35 U.S.C. 103(a) as being unpatentable over Yahata et al., US 6,625,079 B2, in view of Lazar., US 6,771,554 B1.

Regarding claim 1, Yahata teaches that a semiconductor memory comprising:

a memory core (it is taught as a memory circuit MCALL) having a plurality of memory cells (col.3, lines 15-20), a bit line connected to said memory cells, and a sense amplifier connected to said bit line (col.3, lines 28-30);

a command control circuit (Fig.1, it is taught as a signal CT) for outputting an access request signal for accessing said memory cells in response to an access request supplied through a command terminal (col.3, lines 52-54);

a refresh timer (Fig.1, REFTIM) for generating an internal refresh request at predetermined cycles (col.4, lines 6-12);

an arbiter (it is taught as a judgement circuit JUDGE) for determining order of precedence between an access operation corresponding to said access request and a refresh operation corresponding to said internal refresh request (col.7, lines 64 to col.8, lines 7 and lines 59-62) when a conflict occurs between said access request and said internal refresh request (col.8, lines 14-15), and for sequentially outputting a refresh control signal and an access control signal in accordance with the order of precedence (col.8, lines 8-13);

an operation control circuit (it is taught as selector SEL) for making said memory core perform an access operation in response to said access control signal, and making said memory core perform a refresh operation in response to said refresh control signal (col.6,lines 28-41);

Yahata does not teach a detecting circuit for outputting a detection signal indicating that said refresh operation is yet to be performed when a new internal refresh request occurs before said refresh operation corresponding to said internal refresh request is performed, said detecting circuit operating in a test mode.

However, Lazar teaches a detecting circuit for outputting a detection signal (it is taught as address transition detector circuit) indicating that said refresh operation is yet

to be performed when a new internal refresh request occurs before said refresh operation corresponding to said internal refresh request is performed, said detecting circuit operating in a test mode (col.1, lines 30-49).

It would have been obvious to the ordinary skill in the art at the time the invention was made to utilize the teachings of Lazar in the memory system of Yahata and using a detecting circuit for outputting a detection signal indicating that said refresh operation is yet to be performed when a new internal refresh request occurs before said refresh operation corresponding to said internal refresh request is performed because the test mode of operation always precedes an external access cycle with an internal refresh cycle to provide a test operation for test maximum access time delay (col.6, lines 20-23).

According, one of ordinary skill in the art would have recognized this and concluded that they are from the same field of endeavor. This would have motivated one of ordinary skill in the art to implement the above combination for the advantages set forth above.

Regarding claim 2, Lazar teaches further comprising

an external terminal for outputting said detection signal to the exterior of the semiconductor memory (col.4, lines 47 to col.5, lines 3).

Regarding claim 5, Lazar teaches that said refresh timer receives, in said test mode, a refresh adjustment signal for changing the cycle of generation of said internal

refresh request (col.1, lines 64 to col.2, lines 2 and col.5, lines 27-34 and col.8, lines 16-18).

Allowable Subject Matter

9. Claims 6-10 are allowed.

10. Claims 3-4 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Mizugaki et al	US 6842392 B2
Nakashima et al	US 6795363 B2
Lazar	US 6757207 B1
Leung et al	US 6714470 B2
Horiguchi et al	US 6851017 B2
Lazar	Us 6741515 B2

12. When responding to the office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the

art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. 1.111 (c).

13. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jasmine Song whose telephone number is 571-272-4213. The examiner can normally be reached on 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 571-272-4210. The fax phone numbers for the organization where this application or proceeding is assigned are 571-273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Jasmine Song

Patent Examiner

November 2, 2005

FoR

Mano Padmanabhan

Supervisory Patent Examiner

Technology Center 2100

GARY PORTKA
PRIMARY EXAMINER